CLASS TEST

Sl. 01 SK_EE_ABCD_030722 [G]

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ELECTRICAL ENGINEERING

Analog Electronics

Duration : 1:00 hr. **Maximum Marks : 50**

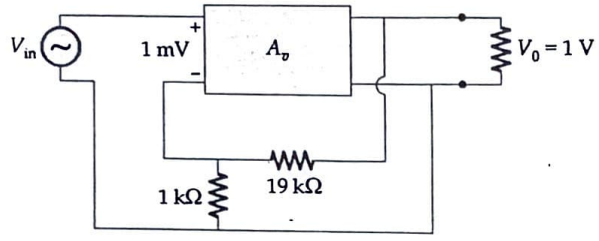
Read the following instructions carefully

1. This question paper contains **30** objective questions. **Q.1-10** carry one mark each and **Q.11-30** carry two marks each.
2. Answer all the questions.
3. Questions must be answered on Objective Response Sheet (**ORS**) by darkening the appropriate bubble (marked **A**, **B**, **C**, **D**) using HB pencil against the question number. Each question has only one correct answer. In case you wish to change an answer, erase the old answer completely using a good soft eraser.
4. There will be **NEGATIVE** marking. For each wrong answer **1/3rd** of the full marks of the question will be deducted. More than one answer marked against a question will be deemed as an incorrect response and will be negatively marked.
5. Write your name & Roll No. at the specified locations on the right half of the **ORS**.
6. No charts or tables will be provided in the examination hall.
7. Choose the **Closest** numerical answer among the choices given.
8. If a candidate gives more than one answer, it will be treated as a **wrong answer** even if one of the given answers happens to be correct and there will be same penalty as above to that questions.
9. If a question is left blank, i.e., no answer is given by the candidate, there will be **no penalty** for that question.

DO NOT OPEN THIS TEST BOOKLET UNTIL YOU ARE ASKED TO DO SO

Q. No. 1 to Q. No. 10 carry 1 mark each

Q.1 Consider the feedback amplifier shown in the figure below:



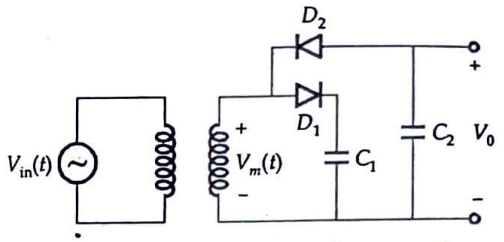
Then the amplifier is a
(a) Voltage amplifier
(b) Current Amplifier
(c) Transresistance Amplifier
(d) Transconductance Amplifier

Q.2 In a centre tap full-wave rectifier, 100 V is the peak voltage between the centre tap and one end of the secondary. What is the maximum voltage across the reverse biased diode?
(a) 200 V (b) 141 V
(c) 100 V (d) 86 V

Q.3 An op-amp with an open loop gain of 1000 V/V is used in the inverting configuration. If in this application, the output voltage ranges from +10 V to -10 V, then the maximum voltage by which the virtual ground node departs from its ideal value is equal to
(a) +10 V from ideal voltage of V_0
(b) +10 mV from ideal voltage of V_0
(c) +10 V from ideal voltage of zero
(d) +10 mV from ideal voltage of zero

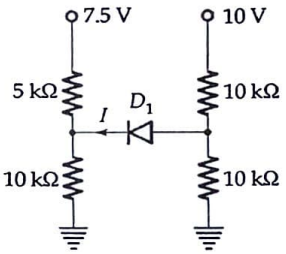
Q.4 A BJT can act as a switch, when it changes from
(a) cut-off to active region
(b) active to saturation region
(c) forward active mode to reverse active mode
(d) saturation to cut-off region

Q.5 Consider the circuit shown in the figure below:



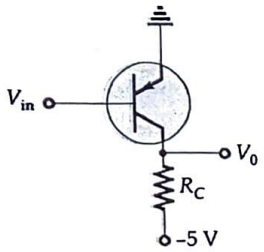
If the value of voltage on the secondary side of transformer is $V_m(t) = V_m \sin(\omega t)$, then the value of V_0 is equal to
(a) $0.5V_m$ (b) $2V_m$
(c) V_m (d) $-V_m$

Q.6 Consider the circuit shown in the figure below



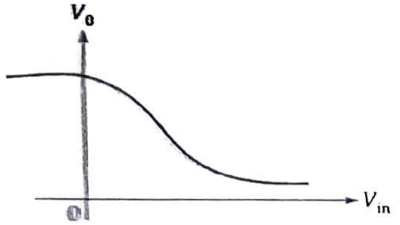
If the cut-in voltage of the diode D_1 is equal to 0.7 V, then the value of current flowing through the diode is
(a) 0 (b) 1 mA
(c) 2 mA (d) 3 mA

Q.7 Consider a *p-n-p* common emitter amplifier shown in the figure below:

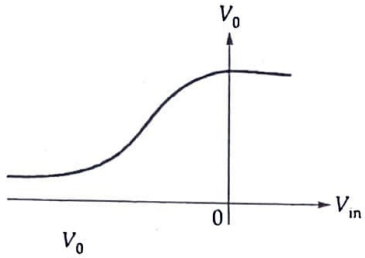


The transfer characteristic of the circuit can be approximately represented as

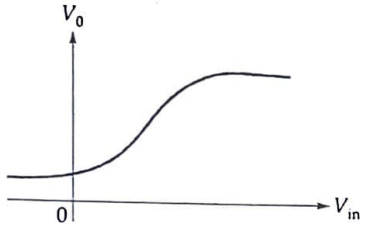
(a)



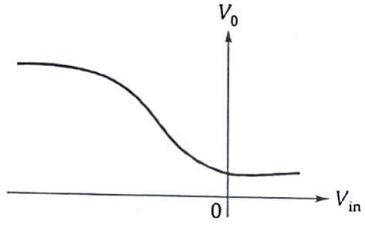
(b)



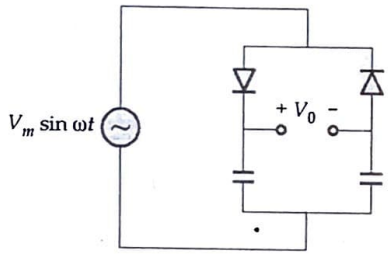
(c)



(d)



Q.8 In the figure shown below, the voltage V_0 is



(a) $|V_m \sin(\omega t)|$ (b) $-2\ V_m$

(c) $-|V_m \sin(\omega t)|$ (d) $2\ V_m$

Q.9 Which of the following statements is **not** correct?

(a) MOSFETs have lower power dissipation than BJTs.

(b) MOSFETs requires lower area for the process of fabrication than BJTs.

(c) MOSFETs are less noise than BJTs.

(d) MOSFETs can drive a larger current than BJTs due to presence of majority carriers only.

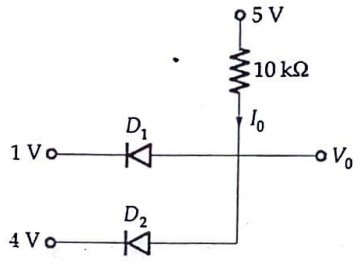
Q.10 A diode whose internal resistance is 40 Ω, is used to supply power to a 1 kΩ load from a 110 V (RMS) source supply. Then the dc load current will be

(a) 149.58 mA (b) 47.61 mA

(c) 42 mA (d) 18.26 mA

Q. No. 11 to Q. No. 30 carry 2 marks each

Q.11 Consider the circuit shown in the figure below:

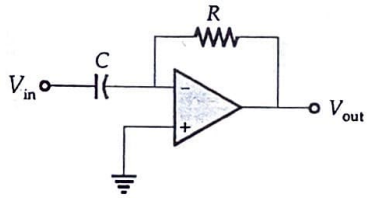


If the diodes D_1 and D_2 are ideal, then the value of V_0 and I_0 are respectively

(a) 1 V and 0.1 mA (b) 4 V and 0.1 mA

(c) 1 V and 0.4 mA (d) 4 V and 0.4 mA

Q.12 Consider the circuit shown in the figure below:



The op-amp is having an open loop finite gain A_0. Rest of the parameters of op-amp is ideal. Then value of pole for the above circuit is located at

(a) $\frac{-A_0}{(RC+1)}$ (b) $-A_0RC$

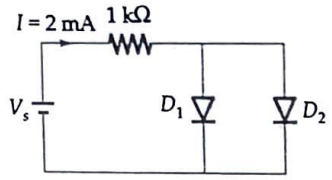
(c) $\frac{A_0}{RC}$ (d) $\frac{-(A_0+1)}{RC}$

Q.13 A negative feedback amplifier with open-loop gain $\frac{A_0}{1+j\frac{\omega}{\omega_0}}$ is connected with a negative feedback circuit with $A_0 > 0$ and feedback factor $\beta(> 0)$. The 3 dB cut-off frequency at which the gain of the resultant feedback circuit reduces by a factor of 0.707 is

(a) $\omega_0 A_0\beta$ (b) $\omega_0(1 + A_0\beta)$

(c) $\omega_0/(1 + A_0\beta)$ (d) $\omega_0(1 - A_0\beta)$

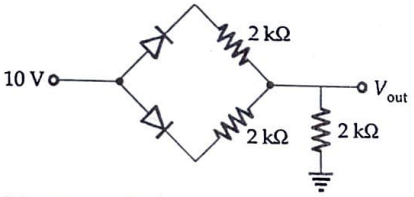
Q.14 Consider the circuit shown in the figure below:



A diode D_1 is connected in parallel with a diode D_2 with reverse saturation current equal to 10^{-12} A and 10^{-10} A respectively. The diodes are connected across a voltage source (V_s) in series with a resistance of 1 kΩ. Then the value of voltage 'V_s' is approximately equal to
(Assuming $\eta = 1$ and $V_{Th} = 26$ mV)

(a) 5.241 V (b) 2.004 V
(c) 2.436 V (d) 4.444 V

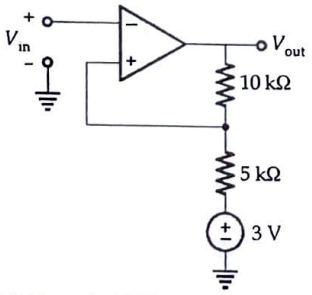
Q.15 In the figure shown below,



The V_{out} of the circuit is _____. (Assume the cut in voltage of the diode $V_\gamma = 0.7$ V)

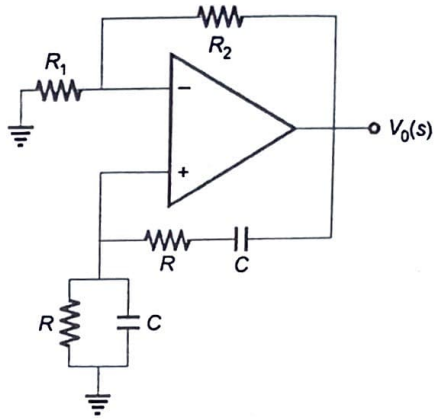
(a) 8.4 V (b) 6.2 V
(c) 9.2 V (d) 0 V

Q.16 For the operational amplifier circuit shown, the output saturation voltage are ±15 V. The upper and lower threshold voltages for the circuit are respectively,



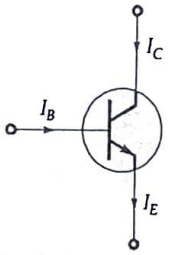
(a) +5 V and –5 V (b) +7 V and –3 V
(c) +3V and –7 V (d) +3 V and –3 V

Q.17 In the following circuit, if the op-amp is ideal, then the minimum required value of the ratio R_2/R_1 to produce sustained oscillations will be



(a) 1 (b) 2
(c) 3 (d) 4

Q.18 Consider the BJT shown below:



Which of the following relation is correct?

(a) $I_C + I_E + \beta I_B = 0$

(b) $I_C = \beta I_B + \dfrac{1}{1+\beta} I_{CO}$

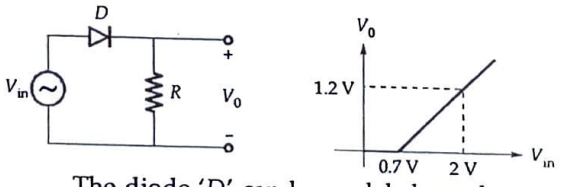
(c) $I_C = \beta I_B + \dfrac{1}{1-\alpha} I_{CO}$

(d) $I_C = \alpha I_B + (1 + \beta) I_{CO}$

Q.19 A Bipolar junction transistor has $\alpha = 0.98$, base current $I_B = 25$ μA and $I_{CBO} = 200$ nA. The emitter current is

(a) 1.05 mA (b) 1.235 mA
(c) 1.33 mA (d) 1.26 mA

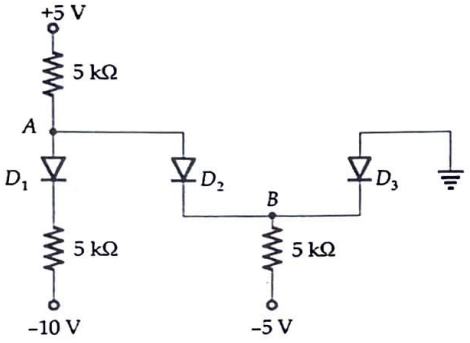
Q.20 Consider the circuit shown in the figure below:



The diode 'D' can be modeled as a battery of voltage V_γ in series with a resistor 'r_f' when biased in forward direction. If the value of resistance $R = 1$ kΩ, then the value of resistance r_f is equal to

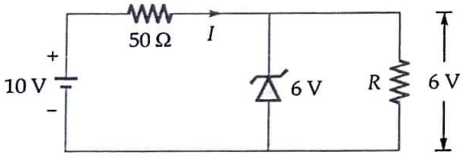
(a) 0.923 Ω (b) 7.133 Ω
(c) 83.33 Ω (d) 101.33 Ω

Q.21 In the diode circuit shown below, the value of voltage V_A is (Assume $V_\gamma = 0.7$ V for each diode)



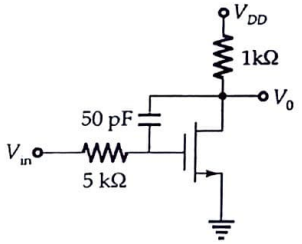
(a) 2 V (b) 0 V
(c) 1.75 V (d) -2.15 V

Q.22 The 6 V zener diode shown below has zero zener resistance and a knee current of 5 mA. The minimum value of R, so that the voltage across it does not fall below 6 V is



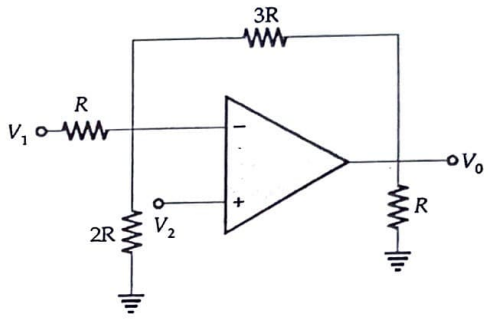
(a) 1.2 kΩ (b) 50 Ω
(c) 80 Ω (d) 0 Ω

Q.23 In the circuit shown below, transistor M1 is in saturation and has transconductance $g_m = 0.01$ S. Ignoring internal parasitic capacitances and assuming the channel length modulation λ to be zero, then the small signal input pole frequency (in kHz) is



(a) 57.87 kHz (b) 75.78 kHz
(c) 87.57 kHz (d) None

Q.24 Assuming that the op-amp in the circuit shown is ideal,

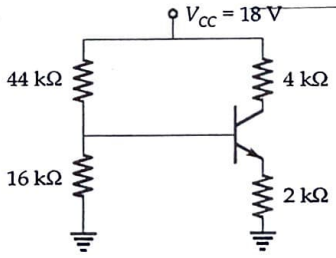


The output voltage V_0 is

(a) $\frac{5}{2}V_1 - 3V_2$ (b) $2V_1 - \frac{5}{2}V_2$

(c) $\frac{-3}{2}V_1 + \frac{7}{2}V_2$ (d) $-3V_1 + \frac{11}{2}V_2$

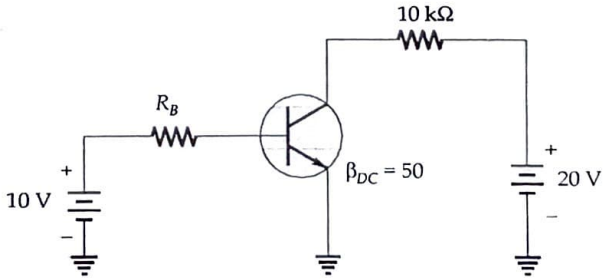
Q.25 Consider the circuit shown in the figure. Assume base-to-emitter voltage V_{BE} = 0.8 V and common-base current gain (α) of the transistor is unity.



The value of the collector-to-emitter voltage V_{CE}

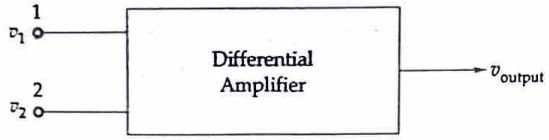
(a) 3 V (b) 4 V
(c) 5 V (d) 6 V

Q.26 In the circuit shown below, the condition to be satisfied such that the silicon transistor will never enter into saturation is (Assume V_{BE} = 0.7 V, $V_{CE\,(sat)}$ = 0 V)



(a) $R_B < 232.5$ kΩ (b) $R_B > 232.5$ kΩ
(c) $R_B < 116.25$ kΩ (d) $R_B > 116.25$ kΩ

Q.27 Consider a differential amplifier as shown below,

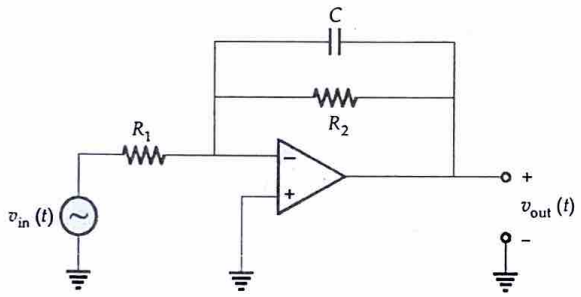


Where the first set of signals is $V_1 = 50\ \mu V$, $V_2 = -50\ \mu V$ and the second set of signals is $V_1 = 1050\ \mu V$, $V_2 = 950\ \mu V$. If the common mode rejection ratio is 100, then the percentage difference in output voltage obtained for the two sets of input signals is

(a) 10% (b) 15%

(c) 20% (d) 25%

Q.28 The op-amp shown in the figure is ideal, $R_1 = 20\ k\Omega$, $R_2 = 40\ k\Omega$ and $C = 10\ \mu F$:



If $V_{in}(t) = 2e^{-2t}\,u(t)$ V and $V_c(0) = 0$, then $V_0(t)$ is

(a) $10\,e^{-2t}\,u(t) + 10\,e^{-2.5t}\,u(t)$

(b) $-20\,e^{-2.5t}\,u(t) + 20\,e^{-2t}\,u(t)$

(c) $-10\,e^{-2t}\,u(t) - 10\,e^{-2.5t}\,u(t)$

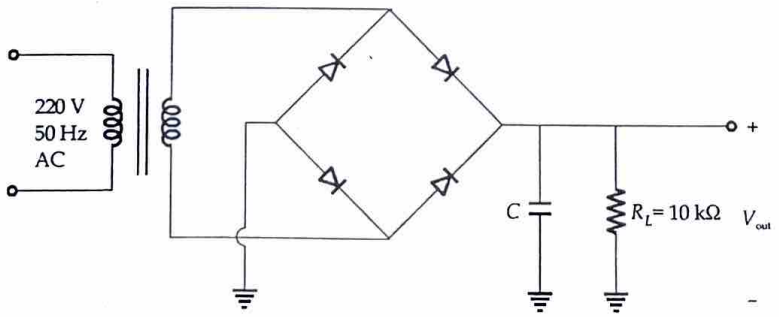
(d) $20\,e^{-2.5t}\,u(t) - 20\,e^{-2t}\,u(t)$

Q.29 For a practical integrator, the component values are $R_1 = 120\ k\Omega$, $R_F = 1.2\ M\Omega$ and the capacitor $C_F = 10$ nF. The dc gain of the integrator is

(a) 10 dB (b) 20 dB

(c) 30 dB (d) 40 dB

Q.30 In the circuit below, a filter capacitor C is used to smooth out the pulses from the full wave rectifier.



The value of capacitor C to maintain the peak to peak ripple voltage as 1% of maximum value of input voltage (V_{max}) is

(a) 10 μF (b) 50 μF

(c) 75 μF (d) 100 μF

■■■■